



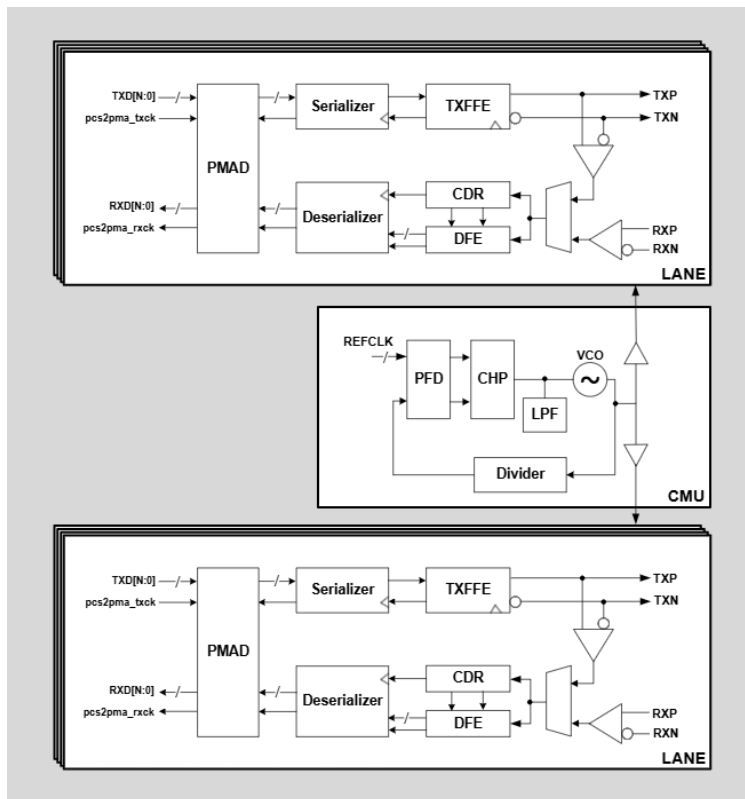
Argos 32Gbps SerDes IP

Overview

The relentless demand for higher data throughput in data centers and high-performance computing (HPC) systems drives the need for ultra-high-speed signaling with minimal latency. **AionChip's Argos SerDes IP** is purpose-built to meet these demands, delivering exceptional signaling bandwidth with industry-leading latency performance.

Leveraging a proven high-speed SerDes architecture, Argos SerDes achieves an optimal balance of latency, power, and area efficiency—without compromising on performance. Its flexible multi-rate design supports data rates from **1.25Gbps to 32Gbps**, ensuring full backward compatibility and seamless integration into next-generation systems.

Key Features



- Modular architecture supporting x1 to x16 lanes with a single CMU
- Lane-based PLL architecture supporting flexible, independent data rates from 1.25 to 32Gbps
- Configurable low latency parallel data interface for optimal system performance
- Broad protocol compatibility including PCIe Gen1–5, Ethernet (1G/10G/25G/50G/100G), JESD204B/C, CPRI, and many other high-speed serial standards
- Adaptive RX EQ combining CTLE + 10-Tap DFE
- Programmable 4-Tap TX FFE with output swing control
- Non-intrusive Eye monitor for real-time signal quality observation
- Comprehensive loopback modes: TX-to-RX, RX-to-TX, Line-side and System-side
- Low-Power Standby State support for energy-efficient operation
- Built-in test and debug features including PRBS Generators and Checkers, AC-JTAG (1149.6), analog debug port



Deliverables

- Standard integration views: LEF abstract view, .LIB timing view, Verilog model, DRC, LVS, ANT reports, and GDSII
- Synthesizable soft RTL with SDC and synthesis script
- Documentations: Datasheet, Integration guide, and Programming guide

Availability

- TSMC 22nm ULP (8 metal layers minimum) – Available now
- TSMC 12nm FFC (9 metal layers minimum) – Under development

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