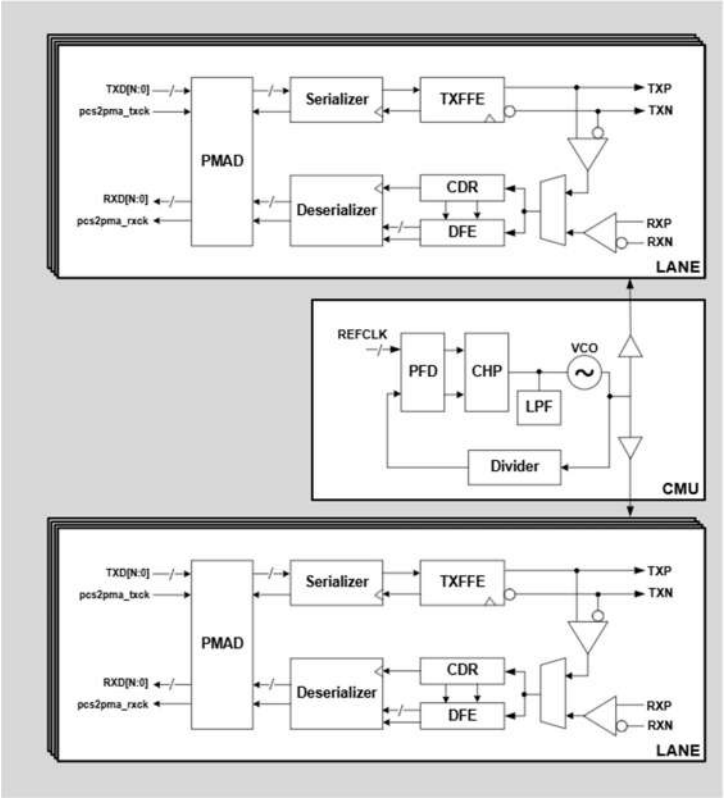
Argos Ultra-Low Latency 32Gbps SerDes IP

Overview

As real-time workloads—from high-frequency trading to low-latency AI and edge analytics—push system responsiveness to the limit, every nanosecond counts. **AionChip's Argos Ultra-Low Latency SerDes IP** delivers ultra-fast signaling with industry-leading performance for the most demanding, mission-critical applications (achieving < 400ps round trip latency at 10Gbps with 2-bit low-latency mode).

Built on a **proven high-speed SerDes architecture**, Argos achieves the **optimal balance of latency, power, and area efficiency** without compromising signal integrity or performance. Its **flexible multi-rate design**, supporting **data rates from 1.25Gbps to 32Gbps**, ensures **backward compatibility** and **seamless deployment** across real-time computing platforms, HPC clusters, and next-generation low-latency networks.

Key Features



- Modular architecture supporting x1 to x16 lanes with a single CMU
- Lane-based PLL architecture supporting flexible, independent data rates from 1.25 to 32Gbps
- Ultra-low latency 2/4/8-bit parallel interface mode for lowest possible latency
- Broad protocol compatibility including PCIe Gen1–5, Ethernet (1G/10G/25G/50G/100G), JESD204B/C, CPRI, and many other high-speed serial standards
- Adaptive RX EQ combining CTLE + 10-Tap DFE
- Programmable 4-Tap TX FFE with output swing control
- Non-intrusive Eye monitor for real-time signal quality observation
- Comprehensive loopback modes: TX-to-RX, RX-to-TX, Line-side and System-side
- Low-Power Standby State support for energy-efficient operation
- Built-in test and debug features including PRBS Generators and Checkers, AC-JTAG (1149.6), analog debug port

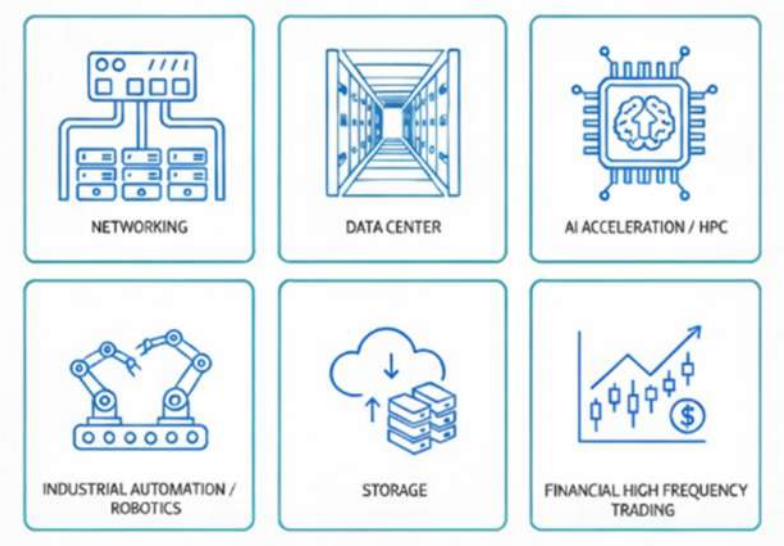
Deliverables

- Standard integration views: LEF abstract view, .LIB timing view, Verilog model, DRC, LVS, ANT reports, and GDSII
- Synthesizable soft RTL with SDC and synthesis script
- Documentations: Datasheet, Integration guide, and Programming guide

Availability

- 22nm (8 metal layers minimum) – Available now
- 12nm (9 metal layers minimum) – Under development

Applications



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